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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,796	03/26/2004	Akinori Haza	61282-068	7166

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/809,796	HAZA ET AL.
	Examiner	Art Unit
	Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-12* is/are pending in the application.

4a) Of the above claim(s) *11 and 12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-7 and 10* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Newly submitted claims 11 and 12 are directed to a method of making a semiconductor device, classified in class 438, subclass 613, that is independent or distinct from the invention originally claimed.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 11 and 12 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 5, 7 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Maruyama (US Pat. 6228684).

Regarding claim 5, Maruyama disclose semiconductor integrated circuit device (ICD) comprising:

- a silicon substrate (11 in Fig. 2)
- a plurality of internal circuits (see 12 in Fig. 1-3) each formed on an element region of the silicon substrate
- a first input/output (I/O) cell formed on an I/O cell region of the silicon substrate (see regions having respective external terminals 14 above the circuit region12 in Fig. 1), the first I/O cell including a first I/O circuit, a first electrode portion (see pad portion 16 connected to wiring 15 in Fig. 1 and 2) horizontally spaced apart from the first I/O circuit with respect to the silicon substrate and a second electrode portion (13A in Fig. 1 and 2) formed on the first I/O circuit and electrically connected to a first internal circuit of the plurality of internal circuits
- a second I/O cell formed on the I/O cell region of the silicon substrate (see region on left side having respective external terminals 14 above the circuit region12 in Fig. 1), the second I/O cell including a second I/O circuit and a third electrode/terminal portion (see 13B in Fig. 2) formed on the second I/O circuit, the third electrode/terminal portion electrically connected to a second internal circuit of the plurality of internal circuits (see 13B and 12 in Fig. 2); and
- a first insulating film/FIF (17 in Fig. 2) formed on the plurality of internal circuits, the first and the second I/O cell and exposing the first electrode/terminal pad as a test/probing electrode/pad (see 16 in Fig. 2),

the second electrode portion as a first terminal pad (see 13A/14 in Fig. 2) and the third electrode portion as a second terminal pad (13B/14 in Fig. 2) (Fig. 1-3; Col. 6, line 60- Col. 9, line 25).

Maruyama further teaches electrically connecting the first electrode/terminal portion and the second electrode/terminal portion to each other through a wiring trace (see 16 and 13 in Fig. 20; Col. 15) and forming a plurality of insulating films on the internal circuits such that the FIF functions as an interlayer insulating film (see 20 and 22 in the structure of Fig. 4).

Regarding claim 7, Maruyama teaches the entire claimed structure as applied to claim 5 above, wherein Maruyama further teaches the internal circuit comprising conventional logic and RAM/SRAM/DRAM circuits (see Col. 12) and including a fuse element (see 24 in Fig. 6; Col. 10, lines 26-60) being electrically connected to the test/probe pad.

Regarding claim 10, Maruyama teaches the entire claimed structure as applied to claim 5 above, wherein Maruyama further teaches the plurality of I/O cells each formed on the respective I/O cell region of the silicon substrate and being placed along one side of the silicon substrate, and wherein each of the plurality of I/O cells is the second I/O cell (see the configuration of 12 on the left and right sides of the substrate in Fig. 1 and 2).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama (US Pat. 6228684).

Regarding claim 6, Maruyama teaches the entire claimed structure as applied to claim 5 above, except an area of each of the first terminal pad and the second terminal pad being smaller than that of the probing pad.

The determination of parameters including size, area, number, etc. of bonding/probe pad/terminal pad, number of terminals/electrodes, width/length of the redistribution wiring etc. in chip packaging and interconnect technology is a subject of routine experimentation and optimization to achieve the desired bonding strength, reliability and test/repair requirement.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the area of each of the first terminal pad and the second terminal pad being smaller than that of the probing pad so that the desired test/repair requirements can be achieved and the reliability can be improved in Maruyama's ICD.

Allowable Subject Matter

6. Claims 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

7. The following is an examiner's statement of reasons for allowance:

The references of record do not teach either singularly or in combination at least the limitations "forming an insulating protective film on a surface of the interlayer insulating film so that the insulating protective film covers the probing pad from the above with respect to the silicon substrate and exposes the first terminal pad and the second terminal pad; forming a rearrangement wiring on a surface of the insulating protective film so that the rearrangement wiring electrically connects to either the first terminal pad or the second terminal pad" and "a solder bump formed on the rearrangement wiring" in a semiconductor integrated circuit device having a plurality of internal circuits each formed on an element region of the silicon substrate including a first and second I/O cells wherein the first and second electrode portions are electrically connected to each other and a third electrode portion is connected to a second internal circuit.

Response to Arguments

7. Applicant's arguments with respect to claims 5-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

09-13-05

NITIN PAREKH

PRIMARY EXAMINER

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